

1 INTERCONNECTIONS FOR FLIP-CHIP USING LEAD-FREE SOLDERS
2 AND HAVING REACTION BARRIER LAYERS
3

4 FIELD OF THE INVENTION
5

6 This invention relates to the interconnection of
7 microelectronic integrated circuit (IC) chips to
8 packages, and in particular area-array flip-chip
9 interconnect technology often called C4 (controlled
10 collapse chip connection). The invention further
11 pertains to interconnection schemes that are
12 environmentally acceptable due to the use of lead-free
13 solder alloys and environmentally benign fabrication
14 processes. Further, the invention pertains to
15 interconnection schemes that eliminate sources of soft
16 errors in on-chip circuitry through the elimination of
17 alpha-particle sources in the solder in contact with
18 the microelectronics circuit.
19

20 BACKGROUND OF THE INVENTION
21

22 In the packaging of semiconductor chips, a hierarchy of
23 interconnections is necessary. At the level of the
24 interconnection between the chip and the substrate (or
25 chip carrier), three different interconnection
26 technologies are widely employed: tape automated
27 bonding (TAB), wire bonding, and area array flip chip
28 interconnect.
29

30 The solder bump area array interconnect scheme is often
31 called a flip-chip solder connection or C4, the
32 face-down soldering of integrated circuit devices (IC)

1 to chip carriers. Unlike wirebonding, the area array
2 solder bump configuration allows the entire surface of
3 the chip to be covered with C4 bumps for the highest
4 possible input/output (I/O) counts to meet the ever
5 increasing demand on the electrical functionality and
6 reliability of the IC technology, than can wire bonding
7 or TAB, which confine the interconnections to the chip
8 periphery.

9
10 More specifically, the C4 technology uses solder bumps
11 deposited on a patterned solder-wettable layered
12 structure known as the ball-limiting metallurgy (BLM),
13 which is also called under bump metallurgy (UBM). UBM
14 defines the terminal metal pads on the top surface of
15 the chip that is wettable by the solder, and which also
16 limits the lateral flow to the pad area. After the
17 solder bumps are reflowed on the patterned UBM pads on
18 the chip to form balls, the chips are joined to a
19 matching footprint of solder-wettable layers on the
20 chip carrier. It is the face-down placement of the
21 chip on the carrier that has led C4 technology to be
22 called flip-chip joining. Compared to other methods of
23 interconnection, the C4 technology offers distinct
24 advantages, including the following: 1) shorter
25 interconnect distances, allowing faster signal response
26 and lower inductance; 2) more uniform power and heat
27 distribution; 3) reduced simultaneous switching noise;
28 and 4) greater design flexibility with the highest
29 possible total input/output counts.
30

1 Fabrication of PbSn C4 interconnections by evaporation
2 through a metal mask has been developed and perfected
3 since the mid-1960s. Both the C4 bumps and BLM pads
4 are evaporated through the patterned metal masks to
5 form a highly reliable, high-density interconnect
6 structure; it has proven extendability from the
7 earliest low density, low Input/output counts IC
8 devices through the high density, high input/output
9 count products of the 2000s. However, it is believed
10 that the limit of extendability to larger wafer sizes,
11 more dense arrays and Pb-free applications has nearly
12 been reached by the evaporation method.

13
14 An alternative method to evaporation is electrochemical
15 fabrication of C4s, which is a selective and efficient
16 process. Electrochemical C4 fabrication has been
17 reported in the literature by, for example, Yung in
18 U.S. Pat. No. 5,162,257, which is incorporated herein
19 by reference. Manufacturability and other integration
20 issues of electrochemically fabricated C4s have been
21 described by Datta, et al. in the J. Electrochem. Soc.,
22 142, 3779 (1995), which is incorporated herein by
23 reference. Using plating and etching processes, and
24 through the development of sophisticated tools, it is
25 possible to obtain a high degree of compositional and
26 volume uniformity of electroplated solders, uniform
27 dimensions of the ball-limiting metallurgy (BLM), and a
28 controlled BLM edge profile.

29

1 The electrochemical process is more extendible to
2 larger wafers and to finer C4 dimensions than the
3 evaporated C4 technology. Electrodeposition through a
4 photoresist mask produces solder only in the mask
5 opening and on top of the UBM. Electrodeposition, in
6 contrast to evaporation, is extendible to high-tin
7 content lead-free alloys and large 300 mm wafers.

8
9 A generic C4 structure consists of all of the elements
10 beginning with the ball-limiting metallurgy
11 (hereinafter the "BLM"). The multi-layer BLM structure
12 generally consists of an adhesion layer, a reaction
13 barrier layer, and a wettable layer to facilitate
14 solder bump joining between the device and the
15 interconnection structure, the chip carriers. The
16 different metal layers in the BLM structure are chosen
17 to be compatible with the solder alloys and with each
18 other, to meet not only stringent electrical,
19 mechanical and reliability requirements in the C4
20 joint, but also to allow easy fabrication.

21
22 A detailed description of the elements comprising the
23 multilayer BLM structure and C4 bumps are summarized
24 as follows.

25
26 1) The first layer to be deposited on the top
27 surface of wafer is the adhesion layer of the BLM which
28 provides adhesion to the underlying substrate. This
29 layer can also serve as a diffusion/reaction barrier
30 layer to prevent any interaction of the silicon wafer
31 and its back-end-of-line (BEOL) wiring layers with the

1 overlying interconnection structure. This is a thin
2 layer typically deposited by sputtering or evaporation
3 on the surface of the wafer passivation layer, which is
4 commonly made of polymer, oxide or nitride materials.
5 Candidates for adhesion layer are Cr, TiW, Ta, W, Ti,
6 TiN, TaN, Zr etc. to just name a few, on the order of
7 hundreds to thousands angstroms in thickness.

8
9 2) The next layer of the BLM is a reaction barrier
10 layer which is solderable by the molten solder but
11 react slowly (limited reaction) to allow for multiple
12 reflow cycles (or rework cycles) without being totally
13 consumed. This layer is typically on the order of
14 thousands of angstroms to microns in thickness.

15
16 3) The final layer of the BLM is the wettable layer,
17 allowing easy solder wettability and fast reaction with
18 solder. A typical example is copper, typically in the
19 range of a few hundreds to thousands of angstroms in
20 thickness, deposited by sputtering, electroless- or
21 electrolytic plating. In some special chip joining
22 applications, Cu thickness can be in the range of
23 microns in thickness.

24
25 4) For the C4 bumps formed on top of the BLM
26 structure, a number of manufacturing processes have
27 been developed that include evaporation, plating,
28 stencil printing, paste screening and solder jetting,
29 and molten solder injection, to name a few.

30

1 5) After formation of the bumps, solder bumps are
2 reflowed. Reflow is done typically in an inert or
3 reducing atmosphere (H_2/N_2) in a belt furnace or in a
4 vacuum furnace or in an oven. During reflow,
5 intermetallic compounds form between solder and the
6 reaction barrier layer. These compounds serve to
7 provide good mechanical integrity for a reliable solder
8 joint.

9
10 6) The wafer is diced into chips, through a dice,
11 sort and pick operation. Good chips (those meeting
12 specifications) are picked and are aligned and flip
13 joined to a chip carrier through the use of a suitable
14 flux or fluxless joining.

15
16 SUMMARY OF THE INVENTION

17
18 It is therefore an aspect of the present invention to
19 provide a BLM structure for flip chip attachment that
20 is suitable for use with and uses a lead free solder.

21
22 It is another object of the invention to provide flip
23 chip electrical connections that reduce the occurrence
24 of soft errors in computer chips.

25
26 The present invention focuses on cost-effective,
27 environmentally sound, reliable BLM for lead-free
28 solders in C4 joints. The present invention also
29 provides the enabling processes for fabrication of an
30 integrated C4 structure, i.e., the selection of the BLM

1 and the deposition and etching processes used to
2 produce the final BLM structure.

3

4 A lead-free C4 typically has Sn as the predominate
5 component, typically greater than 90 wt.%, and one or
6 more alloying elements. Because of the nature of Sn,
7 which is highly reactive, lead-free solders require a
8 more robust reaction barrier layer to protect the
9 terminal metal in the ball-limiting metallurgy and the
10 underlying wiring layers from attack by the Sn-rich
11 solder. The most likely candidates for lead-free
12 solders are tin alloys with a few weight percent of
13 silver, copper, zinc, bismuth, or antimony.

14

15 The elimination of lead from electronic solders is
16 desirable because of the toxicity of lead. The use of
17 lead-free solders also provides a means of limiting the
18 soft errors in circuitry that are caused by alpha
19 particle emission from the solder.

20

21 The solders may be produced by electroplating,
22 evaporation, paste screening or an injection molded
23 solder process which was disclosed in US patents
24 5,244,143; 5,775,569; 6,003,757; and 6,056,191.

25

26 Thus the invention is directed to an interconnection
27 structure suitable for flip-chip attachment of
28 microelectronic device chips to chip carriers, a
29 three-layer ball limiting metallurgy comprising an
30 adhesion layer for deposition on a wafer or substrate;

1 a solder reaction barrier layer of a material selected
2 from the group consisting of Ti, TiN, Ta, TaN, Zr,
3 ZrN, V and Ni; and a solder wettable layer. The
4 adhesion layer may be formed of a material selected
5 from the group consisting of Cr, TiW, TiN, TaN, Ti, Ta,
6 Zr, and ZrN. The solder wettable layer may be formed
7 of a material selected from the group consisting of Cu,
8 Pd, Co, Ni, Au, Pt, and Sn. The interconnection
9 structure may further comprise an optional fourth layer
10 formed of a material selected from the group consisting
11 of Au and Sn, if Au or Sn is not used in the third
12 layer. In one embodiment, the adhesion layer is
13 comprised of one of Cr and TiW, the reaction barrier is
14 comprised of Ti, and the solder wettable layer is
15 comprised of one of Cu, Co, Ni, Pd and Pt.

16
17 The invention is also directed to an interconnection
18 structure suitable for flip-chip attachment of
19 microelectronic device chips to packages, comprising a
20 two-layer ball-limiting composition comprising an
21 adhesion/reaction barrier layer, wherein the
22 adhesion/reaction barrier layer serves both as an
23 adhesion and reaction barrier layer, and a solder
24 wettable layer, the adhesion/barrier layer being for
25 placement between a microelectronic device and the
26 solder wettable layer, and wherein the solder wettable
27 layer is of a metal reactive with components of a
28 tin-containing lead-free solder, so that the solder
29 wettable layer is consumed during soldering, wherein
30 the adhesion/reaction barrier layer remains after being

1 placed in contact with the lead free solder during
2 soldering; and one or more lead-free solder balls are
3 selectively situated on the solder wettable layer, the
4 lead-free solder balls comprising tin as a predominant
5 component and one or more alloying components. The
6 adhesion/reaction barrier layer may be comprised of a
7 material selected from the group consisting of Ti, TiN,
8 TiW, Ta, TaN, Zr, ZrN and V. The solder wettable layer
9 may be comprised of a material selected from the group
10 consisting of Cu, Ni, Co, Pd, Pt, Au and Sn. The
11 interconnection structure may further comprise an
12 optional third layer comprised of Au or Sn, if the
13 second layer is not formed of Au or Sn. Preferably,
14 the lead-free solder ball is comprised of a material
15 that substantially avoids alpha particle emission. The
16 alloying components are selected from the group
17 consisting of Sn, Bi, Cu, Ag, Zn and Sb. The
18 adhesion/reaction barrier layer may comprise Ti and the
19 solderable layer may comprise one of Cu, Co, Ni, Pd and
20 Pt.

21
22 The invention is also directed to an interconnection
23 structure suitable for flip-chip attachment of
24 microelectronic device chips to packages, comprising a
25 three-layer ball-limiting composition comprising an
26 adhesion layer, a reaction barrier layer on top of the
27 adhesion layer and a solder wettable layer, wherein the
28 adhesion/barrier layer is between a microelectronic
29 device and the solder wettable layer and wherein the
30 solder wettable layer is of a composition sufficiently

1 reactive with components of a tin-containing lead free
2 solder, and the reaction barrier layer is substantially
3 less-reactive with solder after being placed in contact
4 therewith in a solder joining process; and one or more
5 lead-free solder balls selectively situated on the
6 solder wettable layer, the lead-free solder balls
7 having tin as a predominant component and one or more
8 alloying components selected from the group consisting
9 of Cu, Zn, Ag, Bi and Sb, whereby the lead-free solder
10 ball substantially avoids alpha particle emission and
11 induced soft logic errors which result therefrom. The
12 solderable layer is formed of a material selected from
13 the group consisting of Cu, Ni, Co, Pd, PdNi, PdCo,
14 NiCo, Au, Pt and Sn.

15
16 The invention is further directed to a method for
17 forming an interconnection structure suitable for
18 flip-chip attachment of microelectronic device chips to
19 packages, comprising forming a ball limiting
20 composition on a substrate; forming a resist pattern on
21 the ball limiting composition; etching the ball
22 limiting composition by using the resist as an etch
23 mask; removing the resist from remaining ball limiting
24 composition; and depositing solder on the ball limiting
25 composition. The solder may be substantially lead
26 free. The ball limiting composition may be formed by
27 depositing an adhesion layer on the substrate;
28 depositing a reaction barrier layer on the adhesion
29 layer; and depositing a solder wettable layer on the
30 barrier layer. The reaction barrier layer may be

1 comprised of a material selected from the group
2 consisting of Ti, TiN, Ta, TaN, Zr, ZnN, V and Ni.
3 The adhesion layer may be deposited by sputtering,
4 plating or evaporating, and may have a thickness of
5 about 100 to about 4000 Angstroms. The reaction
6 barrier layer may also be deposited by sputtering,
7 plating or evaporation, and may have a thickness of
8 about 100 to about 20,000 angstroms. The solder
9 wettable layer also may be deposited by sputtering,
10 plating or evaporation, and have a thickness of about
11 100 to about 20,000 angstroms.

12
13 The method may further comprise depositing a layer
14 comprising Au or Sn on the solder wettable layer. The
15 layer deposited on the solder wettable layer may have a
16 thickness of between substantially 100 to substantially
17 20,000 angstroms, and may be deposited by one of
18 sputtering, electro- or electroless plating or
19 evaporation. The ball limiting composition may be
20 formed by depositing an adhesion/reaction barrier layer
21 on the substrate; and depositing a solder wettable
22 layer on the barrier layer. The method preferably
23 further comprises annealing the ball limiting
24 composition at 150 - 250 degrees C for 30 to 60
25 minutes.

26
27 The invention is also directed to a method for forming
28 an interconnection structure suitable for flip-chip
29 attachment of microelectronic device chips to chip
30 carriers, comprising depositing an adhesion layer on a

1 wafer or substrate serving as the chip carrier;
2 depositing a solder reaction barrier layer on the
3 adhesion layer; depositing a solder wettable layer on
4 the reaction barrier layer; depositing a lead free
5 solder on the solder wettable layer; and reflowing the
6 solder so that the solder wettable layer diffuses into
7 the lead free solder. The solder wettable layer may
8 contain Cu, and the Cu may diffuse into the solder.
9 The lead free solder may be substantially pure Sn, and
10 a binary Sn-Cu lead-free solder is thus formed during
11 reflowing. The lead free solder may substantially
12 binary Sn-Ag, and a ternary Sn-Ag-Cu lead-free solder
13 is thus formed during reflowing. The number of
14 elements in the solder is increased by at least one
15 element, by the diffusion. A eutectic solder may be
16 formed. Preferably, the method further comprises
17 annealing at 150 - 250 degrees C for 30 to 60 minutes.

18
19 The invention also is directed to a method for forming
20 an interconnection structure suitable for flip-chip
21 attachment of microelectronic device chips to chip
22 carriers, comprising depositing an adhesion layer on a
23 wafer or substrate serving as the chip carrier;
24 depositing a solder reaction barrier layer which is
25 solder wettable on the adhesion layer; depositing a
26 lead free solder on the solder wettable layer, and
27 reflowing the solder so that the solder wettable layer
28 diffuses into the lead free solder. The solder
29 wettable layer may contains Cu, and the Cu will thus
30 dissolve into the solder. The lead free solder may be

1 substantially pure Sn, and a binary Sn-Cu lead-free
2 solder is thus formed during reflowing. The lead free
3 solder may be substantially pure Sn-Ag, and a ternary
4 Sn-Ag-Cu lead-free solder thus is formed during
5 reflowing. The number of elements in the solder is
6 increased by at least one element, by the dissolution
7 of the Cu. A eutectic solder may be formed. The
8 method may further comprising annealing at 150 - 250
9 degrees C for 30 to 60 minutes.

10

11 A preferred embodiment of the invention is a three
12 layer BLM structure comprising a Cr adhesion layer on a
13 substrate, a Cu seed layer for plating, and a Ni
14 reaction barrier layer on the Cu layer. It can be a
15 four layer structure when a Cu layer is formed on top
16 of the Ni layer. The top Cu layer may be dissolved into
17 a lead free solder to form a binary Sn-Cu alloy or a
18 ternary Sn-Ag-Cu alloy wherein the solder materials
19 were originally plated as pure Sn and Sn-Ag,
20 respectively, before the incorporation of Cu as an
21 additional element.

22

23 BRIEF DESCRIPTION OF THE DRAWINGS

24

25 These and other aspects, features, and advantages of
26 the present invention will become apparent upon further
27 consideration of the following detailed description of
28 the invention when read in conjunction with the drawing
29 figures, in which:

30

1 FIG. 1 is a cross-sectional view of a first embodiment
2 of C4 structure in accordance with the invention.

3
4 Fig 1A is a cross-sectional view of the embodiment of
5 Fig. 1 after solder reflow.

6
7 FIGS. 2A to 2D show steps in accordance with a first
8 method for forming the C4 structures in accordance with
9 the invention.

10
11 FIGS. 3A to 3D show steps in accordance with a second
12 method for forming the C4 structures in accordance with
13 the invention.

14
15 Fig. 4 is a cross-sectional view of a second embodiment
16 of C4 structure in accordance with the invention.

17
18 Fig 4A is a cross-sectional view of the embodiment of
19 Fig. 4 after solder reflow.

20

21 DESCRIPTION OF THE INVENTION

22

23 Variations described for the present invention can
24 be realized in any combination desirable for each
25 particular application. Thus particular limitations,
26 and/or embodiment enhancements described herein, which
27 may have particular advantages to the particular
28 application need not be used for all applications.
29 Also, it should be realized that not all limitations
30 need be implemented in methods, systems and/or

1 apparatus including one or more concepts of the present
2 invention.
3
4 Referring to Fig. 1, an interconnection structure 10
5 suitable for the connection of microelectronic
6 integrated circuit (IC) chips to packages is provided
7 by this invention. In particular, the invention
8 pertains to the area-array or flip-chip technology
9 often called C4 (controlled collapse chip connection).
10 The BLM (also named an under bump metallurgy (UBM)))
11 is deposited on passivated integrated circuit (IC)
12 device 12 (e.g., a silicon wafer). A first layer of
13 the BLM 11 is an adhesion/diffusion barrier layer 14
14 which may be a metal or compound selected from the
15 group consisting of Cr, W, Ti, Ta, Ta, Ti, V, Zr and
16 their alloys (or compounds), and may have a thickness
17 of about 100 to 4,000 Angstroms, and may be deposited
18 by evaporation, sputtering, electroplating or other
19 known techniques. A solder reaction barrier layer 16
20 of a metal or compound selected from the group
21 consisting of Ti, Ta, Zr, W, V, Ni and their alloys (or
22 compounds) may be subsequently deposited on the
23 adhesion layer, by for example, sputtering, plating, or
24 evaporation to a thickness of about 500 to 25,000
25 Angstroms. Top layer 18 is a solderable layer
26 consisting of a metal selected from the group of Cu,
27 Pd, Pt, Ni, Co, Au, Sn and their alloys, by for example,
28 sputtering, plating, or evaporation to a thickness of
29 about 500 to 10,000 Angstroms. In some special
30 applications, when Cu is used as the wettable layer, a

1 thick Cu layer, in the range of 1-6 microns can be used
2 to form the alloying element with Pb-free solders. An
3 optional fourth layer 38, such a thin layer of gold or
4 Sn, may be deposited on layer 18 to act as a protection
5 layer against oxidation or corrosion, under certain
6 conditions if Au and Sn are not already used in the
7 third layer. With the described layered structure if
8 the selected element is already used in the prior layer
9 it will not be used for the subsequent layer to avoid
10 duplication. Solder 40 is then applied, as shown in
11 Fig. 1.

12
13 The C4 structure 10 may be completed with a lead-free
14 solder ball 20 comprising tin as the predominate
15 component and one or more alloying elements selected
16 from Bi, Ag, Cu, Zn, Ni, Au, In and Sb.

17
18 Example 1 - A three layer UBM

19 In accordance with the present invention, a preferred
20 adhesion layer 14 is Cr, TiW or Ti, , which is
21 preferably either sputtered or evaporated, at a
22 preferred thickness of about 100 to 3000 angstroms. The
23 thickness of the adhesion layer 12 can vary widely as
24 long as both good adhesion and good barrier properties
25 are maintained. If blanket TiW is deposited and
26 subsequently etched as the final step in forming the
27 patterned BLM structure 11, the film thickness should
28 be minimized consistent with adequate performance. An
29 alternative adhesion layer is Cr or Ti at a thickness
30 of about 100 to 3000 angstroms.

1 The second layer 16 is a solder reaction barrier layer,
2 typically a few thousand angstroms to 2 microns in
3 thickness, deposited by sputtering, evaporation or
4 plating. Since the high tin content Pb-free solders
5 are much more reactive than the Pb-rich PbSn solder
6 alloys, Cu, widely used in the high Pb solder, is shown
7 to form thick tin-copper intermetallics at the
8 interface between copper and a high-tin solder and be
9 totally consumed in just few reflow cycles in the
10 thin-film C4 structures, leading to a failure in the
11 integrity of the structure. Thus, a metal other than
12 copper must be used as a solder reaction barrier layer
13 of the BLM in a lead-free C4.

14
15 In accordance with the invention, it has been found
16 that suitable solder reaction barrier layers may be
17 formed of titanium, titanium nitride, tantalum,
18 tantalum nitride, zirconium, zirconium nitride,
19 vanadium or Ni, with Ti being the preferred material.
20 If Ti also adheres well to the device passivation layer
21 then the adhesion and reaction barrier layers can be
22 merged into one layer by the use of Ti.

23
24 The third layer 18 is a solder wettable layer. Layer
25 18 is easily wet by, and potentially totally dissolved
26 into, the molten solder during reflow joining, thus
27 allowing for the formation of a reliable metallurgical
28 joint to the BLM pad through the formation of
29 intermetallics with the reaction barrier layer. The
30 wettable layer is a metal selected from the group

1 consisting of Cu, Pd, Pt, CO, Ni, Sn, Au and their
2 alloys. Both copper and palladium react very rapidly
3 with high-tin alloys and do not provide a suitable
4 reaction barrier layer. However, these metals all
5 react and wet well with solder and therefore serve as
6 the top layer for wetting and joining the C4 solder.

7
8 In an added benefit, Cu dissolving into solder can be
9 used as an alloying element for the solder. For
10 example, when Cu is dissolved into pure Sn solder, it
11 forms the binary Sn-Cu eutectic alloy. When dissolved
12 into binary SnAg alloy, it forms the ternary eutectic
13 Sn-Ag-Cu solder. Both Sn-Cu and Sn-Ag-Cu are the
14 leading Pb-free solder candidates for microelectronic
15 assembly. The dissolution and incorporation of Cu as an
16 added alloying element in solder is shown to
17 particularly simplify the plating processes. Instead
18 of plating a ternary alloy of Sn-Ag-Cu, which is very
19 complicated, a simpler plating of binary SnAg alloy can
20 be performed, with the third element of Cu coming from
21 the BLM pad. The same approach is applied to the
22 plating of pure Sn which is very simple, and the
23 subsequent reaction of pure Sn with Cu, which is from
24 the BLM pad, to form a simple binary alloy. This is
25 much simpler than the plating of a binary Sn-Cu alloy.
26 Maintaining the bath chemistry and precise control of
27 solder composition during the plating of multicomponent
28 solder alloys is very complicated, and this complexity
29 can be avoided using this approach. It is noted that
30 the Cu rapidly diffuses into the essentially liquid

1 solder during the reflow portion of the process, thus
2 assuring that the composition of the solder ball is
3 relatively uniform.

4
5 The manner in which the solder wettable layer is
6 diffused into the solder ball is shown in Fig. 1A for
7 the first embodiment of the invention, and in Fig. 4A
8 for a second embodiment of the invention.

9
10 The solderable layer may be sputtered, evaporated or
11 plated using the same procedure as that used for the
12 deposition of the other BLM layers. Subsequently, the
13 blanket films must be patterned to form the BLM 11 in
14 the finished structure depicted in FIG. 1.

15
16 **Example 2 - A four layer UBM**

17 In this example, the first layer is preferably Cr or
18 TiW. The second layer is preferably Ti, Zr, V, or their
19 alloys (or compounds). The third layer is preferably
20 Cu, CO, Ni, Pd, Pt or their alloys. A fourth layer may
21 be Au or Sn.

22
23 **Example 3 - A simple two layer UBM**

24 In this example, the first layer is preferably Ti which
25 serves both as an adhesion layer and a reaction barrier
26 layer. The second layer is selected from the group
27 consisting of Cu, CO, Ni, Pd, Pt, Sn or their alloys.

28
29 In all three structures Cu is the preferred layer for
30 the reaction, dissolution and incorporation into the

1 solder alloy during reflow joining to form the Sn-Cu or
2 Sn-Ag-Cu solder alloys by simply requiring the plating
3 of the pure Sn or Sn-Ag, respectively, as the bump
4 material.

5
6 The melting properties of the solder alloy that is used
7 over the UBM must be consistent with the requirements
8 of the C4 application. This constraint limits the
9 preferred alloys to those with compositions near the
10 tin-silver eutectic (which contains 2.0-3.8% silver by
11 weight), tin-copper, tin-bismuth, tin-silver-copper
12 ternary eutectic and tin-antimony alloys. The
13 tin-silver eutectic has a melting point of 221 degrees
14 C and is suitable for this application. High-tin
15 tin-copper alloys melt at 227 degrees and tin-bismuth
16 alloys also melt in a suitable range. However, the
17 Sn-Bi phase diagram suggests that alloys with bismuth
18 concentrations approximately 20% by weight will, upon
19 reflow, separate into a tin-rich phase and the
20 tin-bismuth eutectic. For this reason, the preferred
21 embodiment employs tin-bismuth solders with bismuth
22 contents below about 10% by weight. Tin-antimony alloys
23 with antimony contents of less than about 5% by weight
24 also have suitable melting ranges for C4 applications.

25
26 The preferred deposition method for the solder is
27 electrodeposition (either direct electrodeposition of
28 the alloy or sequential deposition of the alloy
29 components), stencil printing or by injection molded
30 solder process or by paste screening.

1 Fig. 2A to Fig 2D illustrate steps in producing the
2 structure of Fig. 1. In Fig. 2A the BLM 11 of Fig. 1,
3 including layers 14, 16 and 18 is produced on a wafer
4 or substrate 12, as explained above. The C4 pattern is
5 defined on the wafer with an appropriate photoresist
6 pattern 24, of thickness at least as great as the
7 thickness of the solder which is to be deposited.

8
9 Referring to Fig. 2B, the lead-free solder 26 is
10 deposited into the resist openings by means of plating,
11 paste screening, stencil printing or molten solder
12 injection, to name a few. Sequential electroplating of
13 the solder components, followed by mixing upon reflow,
14 is an alternative to direct plating of the alloy.

15
16 Referring to Fig. 2C, the resist 24 is removed, by a
17 conventional resist-stripping process. Referring to
18 Fig. 2D the layers 14, 16 and 18 of the BLM 11 are
19 removed , except for regions under the solder 26, by
20 selective electroetching or wet chemical etching, dry
21 etching or a combination of the techniques. The TiW or
22 Cr layer 14 may also be removed by reactive ion
23 etching (RIE) or ion-milling.

24
25 The solder is then reflowed in an appropriate
26 atmosphere to form a solder ball, as illustrated in
27 Fig. 1.

28

1 The wafer 12 may then be diced, sorted, picked and good
2 chips are joined to a ceramic or organic chip carrier
3 employing a suitable flux or by fluxless joining.

4
5 Fig. 3A to Fig. 3D illustrate an alternative process to
6 form the structure of Fig. 1. In Fig. 3A, a photoresist
7 pattern 24, is deposited over the blanket BLM 11. Fig.
8 3B illustrates the etching of the layers of the BLM 11
9 which is not covered under the photoresist 24. The
10 photoresist pattern 24 being used as an etch mask to
11 pattern the BLM. In Fig. 3C, the photoresist pattern
12 24 is stripped off the patterned BLM layers. In Fig.
13 3D, the solder bumps are selectively deposited on the
14 BLM 11 by means of paste screening, molten solder
15 injection, stencil printing, electroless and
16 electrolytic plating, etc.

17
18 The solder bump 26 is then reflowed in an appropriate
19 atmosphere.

20
21 The wafer is then diced, sorted and picked. Good chips
22 are selected and joined to a chip carrier either with a
23 suitable flux or fluxlessly joined.

24
25 Fig. 4 is a cross-sectional view of a second embodiment
26 of C4 structure in accordance with the invention. The
27 BLM 30 is a two layer structure suitable for deposition
28 on a substrate or wafer with oxide, nitride or
29 polyimide passivation 32. The first layer 34, which is
30 deposited on the surface of the passivated wafer or

1 substrate may be Cr, Ti, Ta, Zr, V or their alloys. The
2 next layer 36 serves as a solderable layer, is
3 deposited on the layer 34, and may be selected from the
4 group of Cu, Pd, Pt, Co, Ni, Sn. Layer 36 should be a
5 material other than that already selected for the first
6 layer. An optional third layer 38, such as a thin
7 layer of gold or Sn, may be deposited on layer 36 to
8 act as an oxidation protection layer. Solder 40 is then
9 applied, as in Fig. 1.

10

11 As noted above, when the optional layer 38 is not
12 applied and the top layer of Fig. 4 is, for example Cu,
13 the manner in which the solder wettable layer is
14 dissolved into the solder ball 40 is shown Fig. 4A.

15

16 The embodiment illustrated in Fig. 4 may be formed
17 using either one of the methods illustrated in Fig. 2A
18 to Fig. 2D or in Fig. 3A to Fig. 3D.

19

20 Example 4 - A two layer UBM

21 The first layer is preferably Ti or its alloys, with Ti
22 serving both as an adhesion and reaction barrier metal.
23 The second layer above this layer is selected from the
24 group consisting of Cu, Co, Ni, Pd, Sn and Pt.

25

26 Example 5 - A three layer BML structure

27 A three layer BLM structure comprising a Cr adhesion
28 layer deposited on a substrate, a Ni reaction barrier
29 layer on the Cr layer, and a Cu seed layer for plating
30 deposited on the Cr layer. A lead free solder of Sn, or

1 an SnAg alloy is deposited on the Cu layer. When
2 reflowed, as described above, the Cu layer is dissolved
3 into the resulting solder ball to alloy with the
4 solder. The solder is preferably lead-free, and a
5 binary Sn-Cu alloy or a ternary Sn-Ag-Cu alloy is
6 formed when the Cu is dissolved into the solder wherein
7 the original solders were pure Sn and binary Sn-Ag,
8 respectively.

9

10 Example 6

11 A four layer structure comprising a Cr adhesion layer
12 for deposit on a substrate, a Cu layer on the Cr layer,
13 a Ni reaction barrier layer on the Cu layer, a layer of
14 Cu on top of the Ni layer. Upon reflow of a plated pure
15 Sn or binary Sn-Ag solder, the top layer of Cu
16 dissolves into the lead-free solder to form a binary
17 Sn-Cu alloy or a ternary Sn-Ag-Cu alloy, respectively.

18

19 The BLM metallurgy of the present invention may be
20 further improved in robustness by annealing at 150 -
21 250 degrees C for 30 to 60 minutes after BLM
22 patterning.

23

24 Thus, while there have been shown and described and
25 pointed out fundamental novel features of the invention
26 as applied to currently preferred embodiments thereof,
27 it will be understood that various omissions,
28 substitutions and changes in the form and details of
29 the method and product illustrated, and in their
30 operation, may be made by those skilled in the art

1 without departing from the spirit of the invention. In
2 addition it is to be understood that the drawings are
3 not necessarily drawn to scale. It is the intention,
4 therefore, to be limited only as indicated by the scope
5 of the claims appended herewith and equivalents
6 thereof.

7
8 It is noted that the foregoing has outlined some of the
9 more pertinent objects and embodiments of the present
10 invention. The concepts of this invention may be used
11 for many applications. Thus, although the description
12 is made for particular arrangements and methods, the
13 intent and concept of the invention is suitable and
14 applicable to other arrangements and applications. It
15 will be clear to those skilled in the art that other
16 modifications to the disclosed embodiments can be
17 effected without departing from the spirit and scope of
18 the invention. The described embodiments ought to be
19 construed to be merely illustrative of some of the more
20 prominent features and applications of the invention.
21 Other beneficial results can be realized by applying
22 the disclosed invention in a different manner or
23 modifying the invention in ways known to those familiar
24 with the art. Thus, it should be understood that the
25 embodiments has been provided as an example and not as
26 a limitation. The scope of the invention is defined by
27 the appended claims.

28